



Over 30 Years of Quality Through Innovation

LSJ689
LOW NOISE LOW CAPACITANCE
MONOLITHIC DUAL
P-CHANNEL JFET AMPLIFIER

FEATURES	
ULTRA LOW NOISE	$e_n = 2.0nV/\sqrt{Hz}$
LOW INPUT CAPACITANCE	$C_{iss} = 8pF$

Features

- Reduced Noise due to process improvement
- Monolithic Design
- High slew rate
- Low offset/drift voltage
- Low gate leakage I_{gss} & I_g
- High CMRR 102 dB

Benefits

- Tight differential voltage match vs. current
- Improved op amp speed settling time accuracy
- Minimum Input Error trimming error voltage
- Lower intermodulation distortion

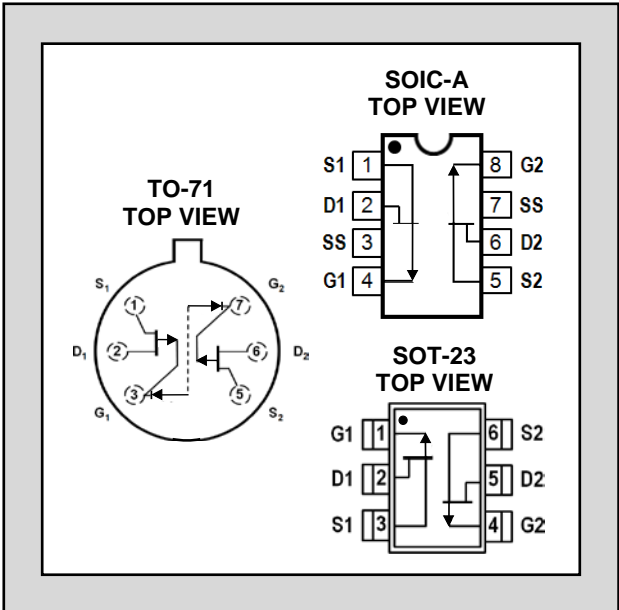
Applications

- Wide band differential Amps
- High speed temperature compensated single ended input amplifier amps
- High speed comparators
- Impedance Converters

Description

The LSJ689 high performance, P-Channel, monolithic dual JFET features extremely low noise, tight offset voltage and low drift over temperature. It is targeted for use in a wide range of precision instrumentation applications. The SOT-23, TO-71 and SO-8 packages provide ease of manufacturing and the symmetrical pinouts prevent improper orientation. The SOT-23 and SO-8 packages are available in tape and reel, compatible with automatic assembly methods. (See packaging data)

ABSOLUTE MAXIMUM RATINGS ¹ @ 25 °C (unless otherwise stated)	
Maximum Temperatures	
Storage Temperature	-55 to +150°C
Junction Operating Temperature	-55 to +150°C
Maximum Power Dissipation, TA = 25°C	
Continuous Power Dissipation, per side ⁴	300mW
Power Dissipation, total ⁵	500mW
Maximum Currents	
Gate Forward Current	$I_{G(F)} = -10mA$
Maximum Voltages	
Gate to Source	$V_{GS} = 50V$
Gate to Drain	$V_{GD} = 50V$



MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$ V_{GS1} - V_{GS2} $	Differential Gate to Source Voltage			20	mV	$V_{DS} = -15V, I_G = -1mA$
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.90		1.0		$V_{DS} = -15V, V_{GS} = 0V$
CMRR	COMMON MODE REJECTION RATIO $-20 \log \Delta V_{GS1-2}/\Delta V_{DS} $	95	102		db	$V_{DS} = -10V \text{ to } -20V, I_D = -200\mu A$

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
e_n	Noise Voltage		1.9		nV/ \sqrt{Hz}	$V_{DS} = -15V, I_D = -2.0mA, f = 1kHz, NBW = 1Hz$
e_n	Noise Voltage		2.2		nV/ \sqrt{Hz}	$V_{DS} = -15V, I_D = -2.0mA, f = 100Hz, NBW = 1Hz$
C_{ISS}	Common Source Input Capacitance		8		pF	$V_{DS} = -15V, I_D = -200\mu A, f = 1MHz$
C_{RSS}	Common Source Reverse Transfer Capacitance		3		pF	

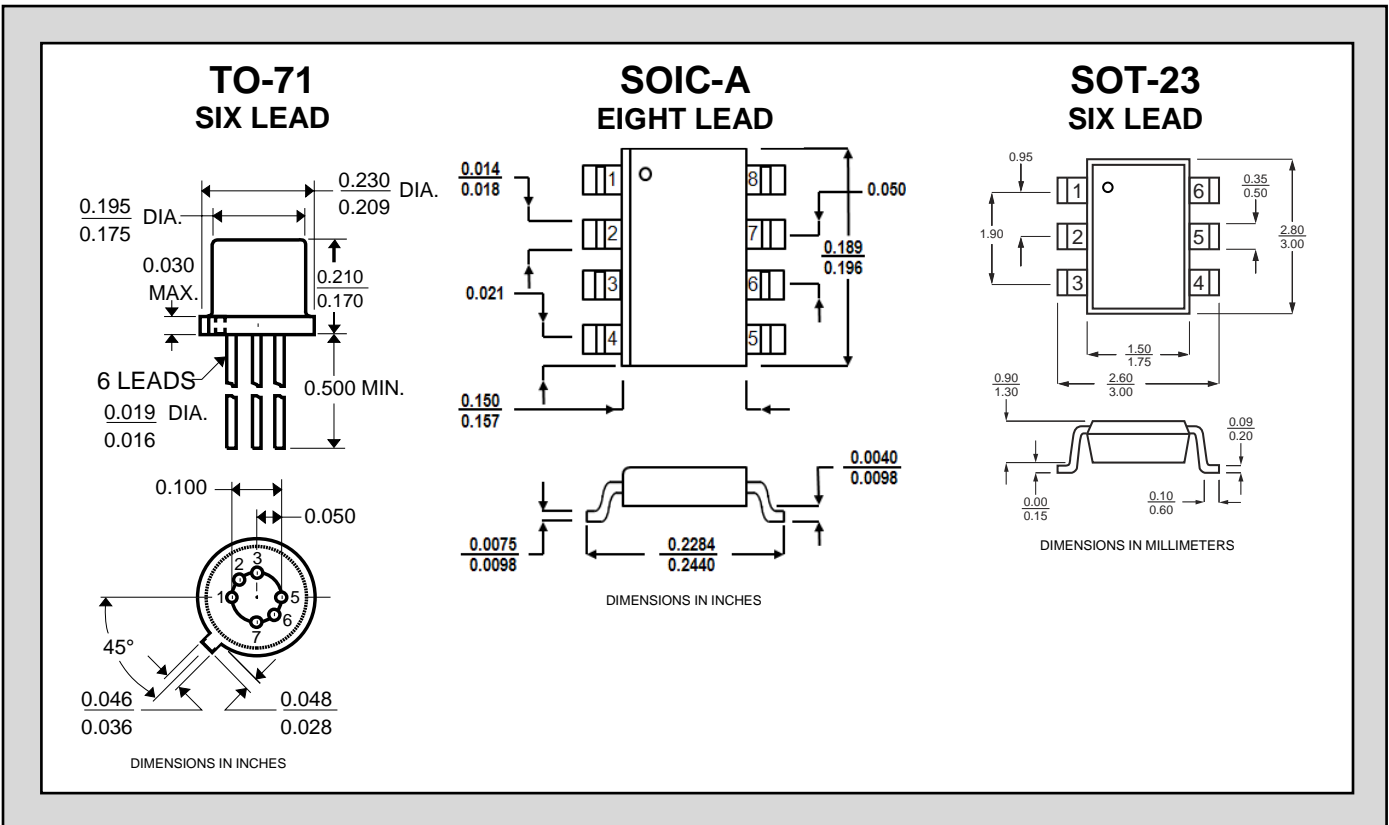
ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	50			V	$V_{DS} = 0V, I_G = 1\mu A$
$V_{(BR)G1-G2}$	Gate to Gate Breakdown Voltage	± 30	± 45		V	$I_G = \pm 1\mu A, I_D = I_S = 0A$ (Open Circuit)
$V_{GS(OFF)}$	Gate to Source Pinch-off Voltage	1.50		5.0	V	$V_{DS} = -15V, I_D = -1nA$
I_{DSS}^2	Drain to Source Saturation Current	-2.5		-30	mA	$V_{DS} = -15V, V_{GS} = 0V$
I_G	Gate Operating Current		2		pA	$V_{DG} = -15V, I_D = -200\mu A$
I_{GSS}	Gate to Source Leakage Current		0.9	100	pA	$V_{GS} = 15V, V_{DS} = 0V$
G_{fs}	Full Conductance Transconductance	1500			μS	$V_{DS} = -15V, V_{GS} = 0V, f = 1kHz$
G_{fs}	Transconductance		1500		μS	$V_{DS} = -15V, I_D = -200\mu A, f = 1kHz$
G_{OS}	Full Output Conductance		38		μS	$V_{DS} = -15V, V_{GS} = 0V, f = 1kHz$
G_{OS}	Output Conductance		3		μS	$V_{DS} = -15V, I_D = -200\mu A, f = 1kHz$
NF	Noise Figure		0.5		db	$V_{DS} = -15V, V_{GS} = 0V, R_G = 10m\Omega$

TYPICAL SPICE PARAMETERS FOR LSJ689 IN LT SPICE FORMAT:

LSJ689_4 IDSS = 14.0mA RDS=112
.MODEL LSJ689_4 PJF (LEVEL=1 BETA=28E-4 VTO=-2.75 LAMBDA=2E-3
+ IS=4.5E-16 N= 1 RD=73 RS=35 CGD=6E-12 CGS=11E-12 PB=0.25 MJ=0.3 FC=0.5
+ KF=2E-18 AF=1 XTI=0)

PACKAGE DIMENSIONS

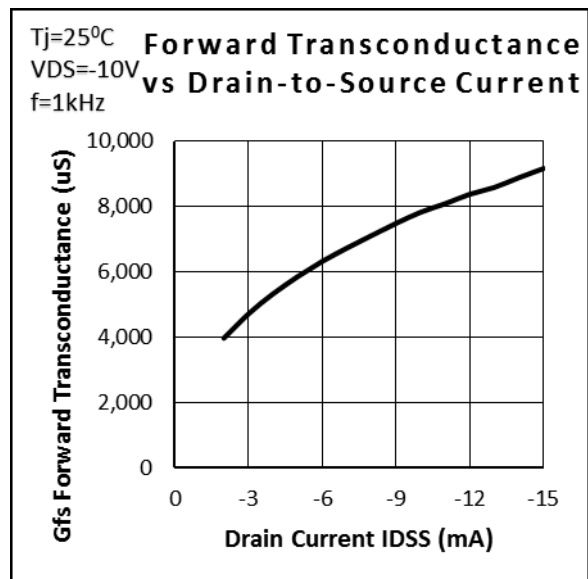
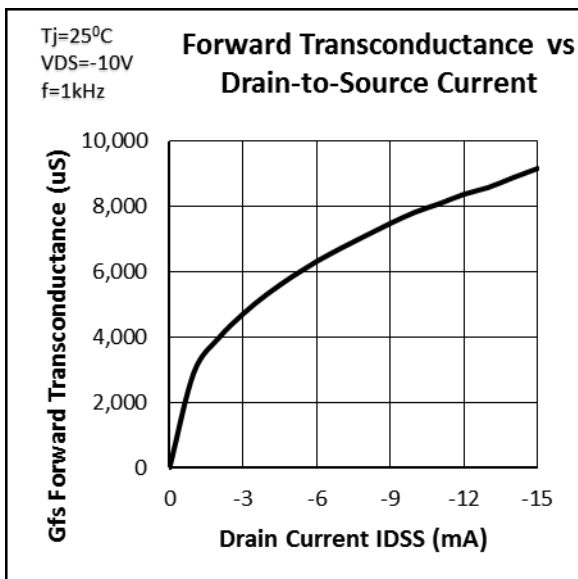
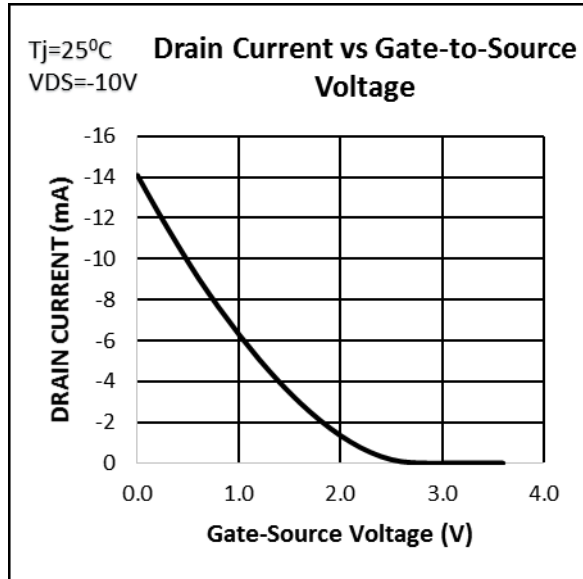
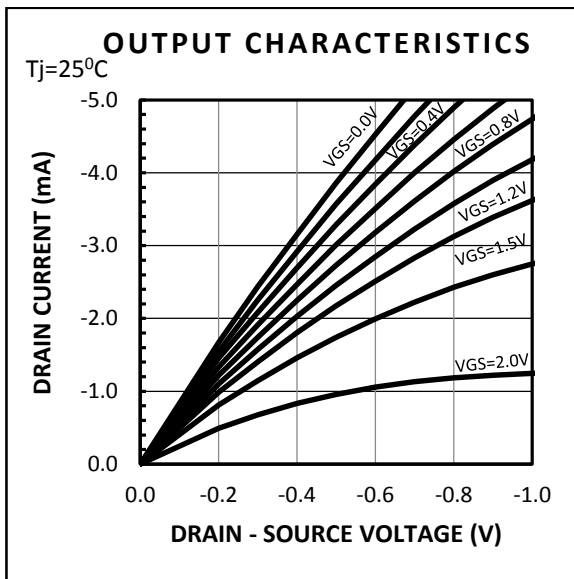
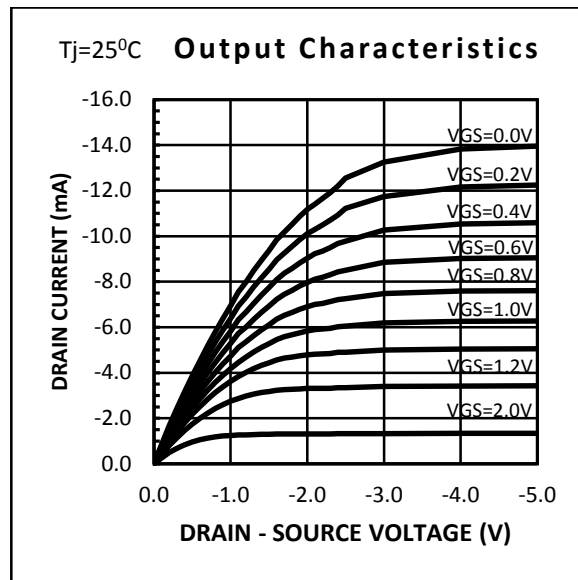
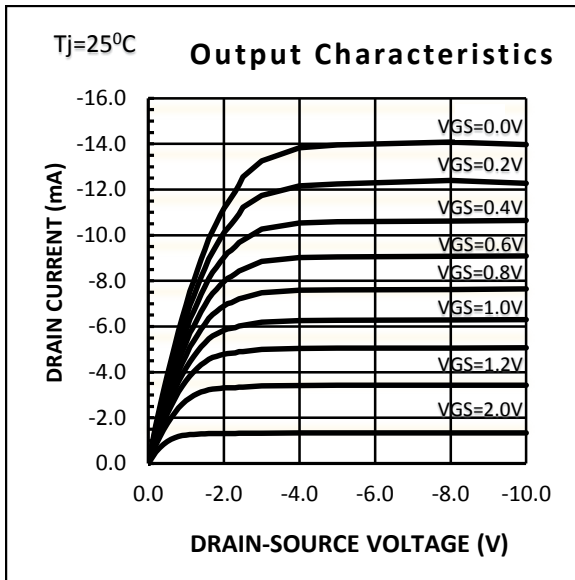


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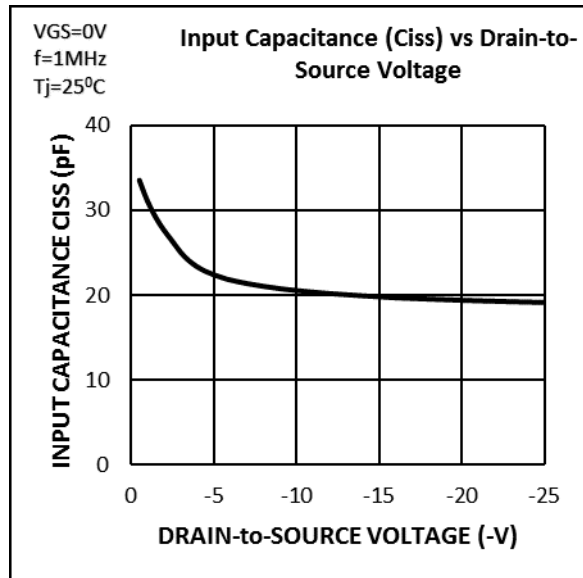
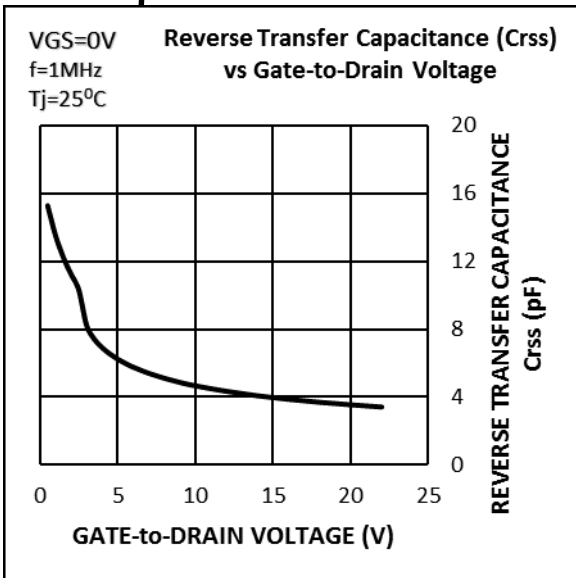
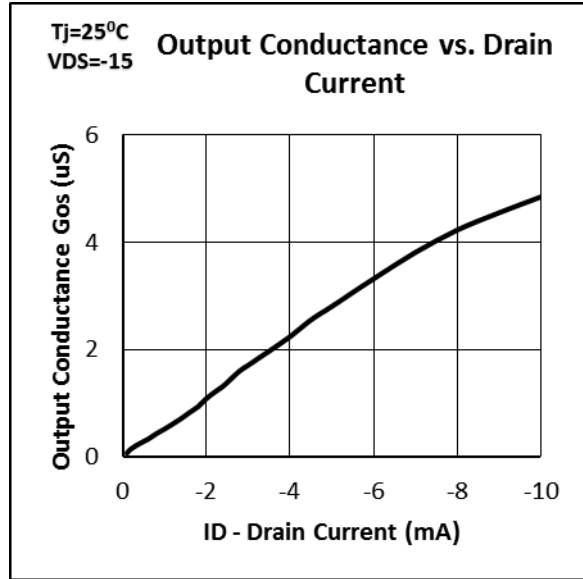
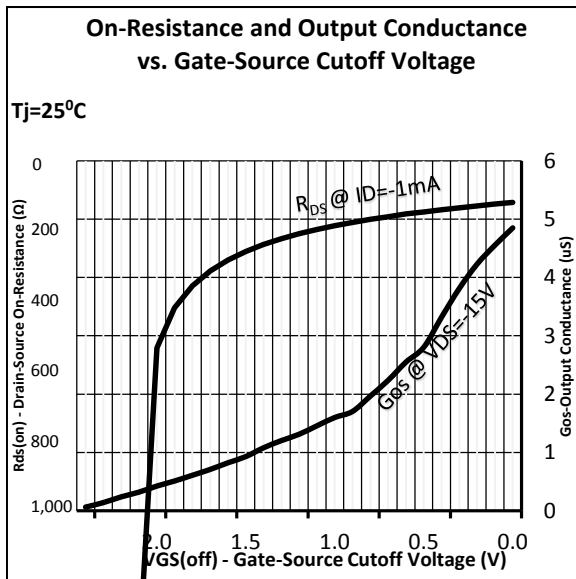
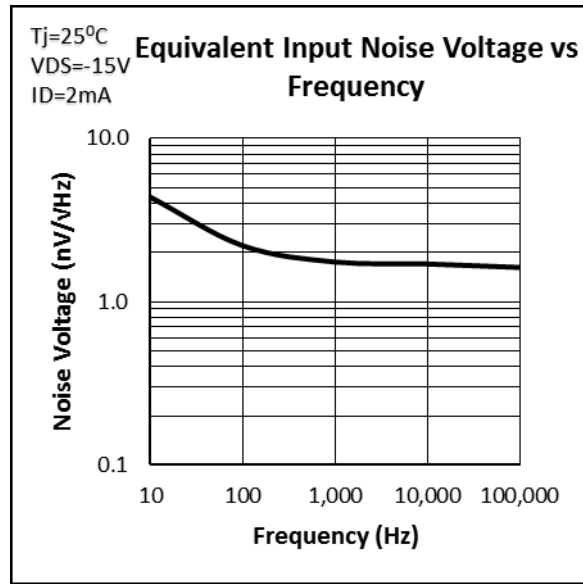
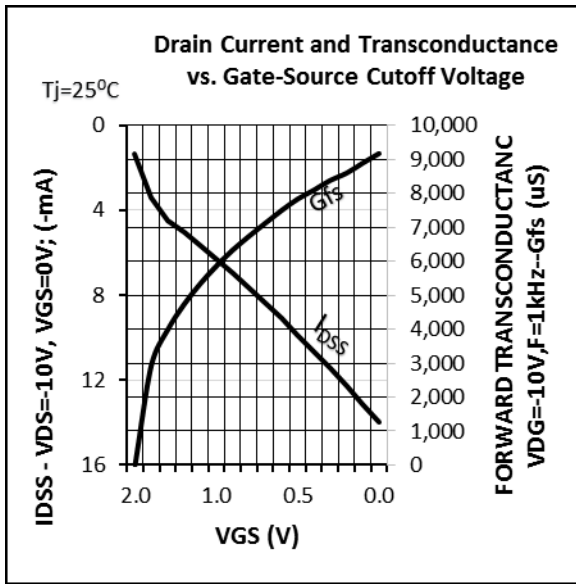
1. Absolute maximum ratings are limiting values above which serviceability may be impaired.
2. Pulse width $\leq 2_{ms}$.
3. All MIN/TYP/MAX Limits are absolute values. Negative signs indicate electrical polarity only.
4. Derate 2.4 mW/°C above 25°C.
5. Derate 4 mW/°C above 25°C.

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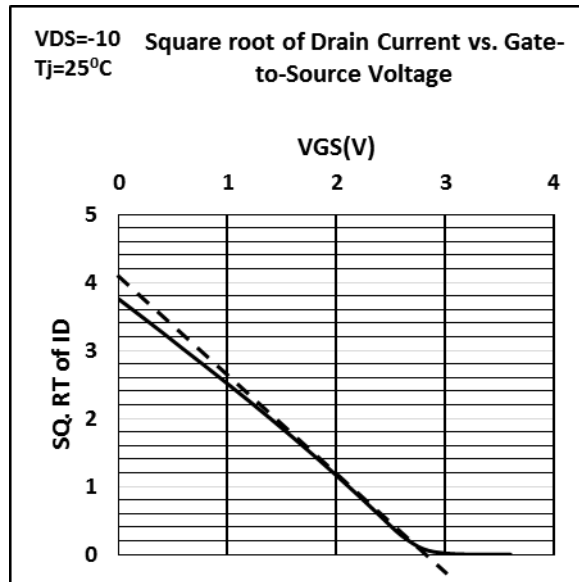
TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (CONT'D)



TYPICAL CHARACTERISTICS (CONT'D)



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